CLAIMS

What is claimed is:

1. A digital clock manager having a reference input terminal, a skew input terminal, an output terminal, and a frequency adjusted output terminal, the digital clock manager comprising:

a delay lock loop (DLL) coupled to the reference input terminal, the skew input terminal, and the output terminal; and

a digital frequency synthesizer, coupled to the delay lock loop and the frequency adjusted output terminal.

2. The digital clock manager of Claim 1, wherein the delay lock loop is configured to generate an output clock signal on the output terminal which synchronizes a reference clock signal on the reference input terminal with a skewed clock signal on the skew input terminal.

3. The digital clock manager of Claim 1, wherein the digital frequency synthesizer is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal and wherein the frequency adjusted clock signal is synchronized with the output clock signal during concurrences.

4. The digital clock manager of Claim 1, wherein the delay lock loop comprises a DLL output circuit having a DLL output delay.

5. The digital clock manager of Claim 4, wherein the digital frequency synthesizer comprises a DFS output circuit having a DFS output delay.

6. The digital clock manager of Claim 5, wherein the DLL output delay is substantially equal to the DFS output delay.

7. The digital clock manager of Claim 5, wherein the DLL output circuit comprises a plurality of components and the DFS output circuit comprises the same plurality of components.

8. The digital clock manager of Claim 1, wherein the delay lock loop drives a synchronizing clock signal to the digital frequency synthesizer.

9. The digital clock manager of Claim 8, wherein the delay lock loop is configured to generate an output clock signal on the output terminal, wherein the output clock signal lags the synchronizing clock signal by a DLL output delay.

10. The digital clock manager of Claim 9, wherein the digital frequency synthesizer is configured to generate a frequency adjusted clock signal on the frequency adjusted output terminal, wherein an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by a DFS output delay during a concurrence period.

11. The digital clock manager of Claim 10, wherein the DLL output delay is substantially equal to the DFS output delay.

12. The digital clock manager of Claim 1, further comprising a variable delay circuit coupled between the delay lock loop and the output terminal.

13. The digital clock manager of Claim 1, further comprising a variable delay circuit coupled between the digital frequency synthesizer and the frequency adjusted output terminal.

14. The digital clock manager of Claim 1, further comprising a multiplexer having a first input terminal coupled to the reference input terminal, a second input terminal coupled to the delay lock loop, and an output terminal coupled to the digital frequency synthesizer.

15. The digital clock manager of Claim 1, wherein the delay lock loop is configured to provide a synchronizing clock signal to the second input terminal of the multiplexer.

16. The digital clock manager of Claim 15, wherein the digital frequency synthesizer is configured to perform a frequency search phase using a reference clock signal provided to the reference input terminal.

17. The digital clock manager of Claim 16, wherein the digital frequency synthesizer is configured to provide a frequency adjusted clock signal based on the synchronizing clock signal.

18. The digital clock manager of Claim 1, wherein the digital frequency synthesizer performs a frequency search while the delay lock loop is performing lock acquisition.

19. A method to generate an output clock signal and a frequency adjusted clock signal from a reference signal, wherein the output clock signal is synchronized with the frequency adjusted clock signal during a concurrence; the method comprising:

generating a synchronizing clock signal;

matching a DLL output delay with a DFS output delay;

generating the output clock signal lagging the synchronizing clock signal by the DLL output delay; and

generating the frequency adjusted clock signal so that an active edge of the frequency adjusted clock signal lags an active edge of the synchronizing clock signal by the DFS output delay during the concurrence.

20. The method of Claim 19, wherein the step of matching a DLL output delay with a DFS output delay comprises synchronizing a DLL output circuit with a DFS output circuit.

21. The method of Claim 19, further comprising performing lock acquisition.

22. The method of Claim 21, further comprising performing a frequency search during lock acquisition.